UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KI-YOUNG LEE and SEOK-WOO HONG

Appeal No. 2005-2055
Application No. 09/389,491

ON BRIEF

Before HAIRSTON, RUGGIERO, and LEVY, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 12, 14-24, and 26, which are all of the claims pending in the present application. An amendment filed May 12, 2003 after final rejection was approved for entry by the Examiner.

The claimed invention relates to a method of manufacturing a semiconductor integrated circuit capacitor in which first and

second via holes are formed simultaneously. More particularly, the first via hole, in the capacitor formation part of the circuit structure, and the second via hole, in the wire line formation part of the circuit structure, are simultaneously formed when a dielectric layer over exposed surfaces is formed and etched. The formation of the dielectric layer further results in the side profile of the first via hole sloping slightly through use of a sloping spacer made of conductive layer material. According to Appellants (Specification, page 11), the described method overcomes the dielectric disconnection problem of conventional capacitor manufacturing methods caused by undercutting of the lower electrode.

Claim 12 is illustrative of the invention and reads as follows:

> 12. A method of manufacturing a semiconductor integrated circuit capacitor, comprising:
>
> providing an insulating substrate;
>
> simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating substrate;
>
> forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes, including on the exposed predetermined surfaces of the lower electrode and first wire line;

performing a tungsten etch back process to selectively etch back the tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes to simultaneously form: (i) a tungsten containing conductive sidewall spacer on the sidewalls of the first via hole and a portion of the exposed predetermined surface of the lower electrode from the tungsten containing conductive layer formed in the first via hole for preventing dielectric disconnection; (ii) a tungsten containing conductive plug in the second via hole on the predetermined surface of the first wire line from the tungsten containing conductive layer formed in the second via hole, the tungsten containing conductive sidewall spacer and the tungsten containing conductive plug being formed of the same tungsten containing conductive layer; and (iii) an exposed surface containing the spacer, conductive plug, a portion of the predetermined surface of the lower electrode not covered by the tungsten containing conductive sidewall spacer, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the tungsten containing conductive sidewall spacer and the tungsten containing conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer

disposed on the tungsten containing conductive sidewall spacer, and predetermined surface of the lower electrode not covered by the tungsten containing conductive sidewall spacer; and

simultaneously forming: (i) a second wire line connected to the tungsten containing

conductive plug; and (ii) an upper electrode connected to the dielectric layer.

The Examiner relies on the following prior art:

Kuwajima	5,534,461	Jul. 09, 1996
Nulty et al. (Nulty)	6,066,555	May 23, 2000 (filed Dec. 22, 1995)
Oh et al. (Oh)	6,074,907	Jun. 13, 2000 (filed Apr. 29, 1998)
Gambino et al. (Gambino)	6,166,423	Dec. 26, 2000 (effectively filed Jan. 15, 1998)

Claims 12, 14-24, and 26, all of the appealed claims, stand finally rejected under 35 U.S.C. § 103(a). As evidence of obviousness, the Examiner offers Gambino in view of Kuwajima with respect to claims 12, 14-16, 18-22, 24, and 26, adds Oh to the basic combination with respect to claim 17, and adds Nulty to the basic combination with respect to claim 23.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs[1] and Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection, and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 12, 14-24, and 26. Accordingly, we affirm.

[1] The Appeal Brief was filed February 17, 2004. In response to the Examiner's Answer mailed November 15, 2004, a Reply Brief was filed January 14, 2005, which was acknowledged and entered by the Examiner as indicated in the communication mailed February 1, 2005.

At the outset, we note that Appellants indicate (Brief, page 5) that the appealed claims stand or fall together as a group. Consistent with this indication, Appellants' arguments in the Briefs are directed solely to features which are set forth in independent claim 1. Accordingly, we will select independent claim 1 as the representative claim for all the claims on appeal, and claims 14-24, and 26 will stand or fall with claim 1. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983). Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed waived (see 37 CFR § 41.37(c)(1)(vii)).

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the

relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

With respect to representative independent claim 1, Appellants' arguments in response to the Examiner's 35 U.S.C. § 103(a) rejection assert a failure to establish a prima facie case of obviousness since proper motivation for the Examiner's proposed combination of the Gambino and Kuwajima references has not been established. In particular, Appellants contend (Brief, pages 11 and 12; Reply brief, page 2) that there is no teaching in the Kuwajima reference, relied upon by the Examiner as providing a teaching of using a sidewall spacer, that the tungsten sidewall spacer 14c is intended to correct a dielectric disconnection problem as claimed. According to Appellants (id.), Kuwajima is not concerned with dielectric disconnection since the tungsten layer 14 does not rest on a dielectric layer, but rather on a barrier metal layer 13a, 13b.

After reviewing the applied prior art references in light of the arguments of record, however, we are in general agreement with the Examiner's position as stated in the Answer. Although Appellants contend that no inducement exists for combining Gambino with Kuwajima, we would point out that it is not necessary that references be combined for the same reason as Appellants. The reason or motivation to modify a reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the same advantage or result discovered by Appellants. See In re Lintner, 458 F.2d 1013, 1015-16, 173 USPQ 560, 562 (CCPA 1972); In re Dillon, 919 F.2d 688, 692, 16 USPQ2d 1897, 1901 (Fed. Cir. 1990)(en banc), cert. denied, 500 U.S. 904 (1991).

As articulated by the Examiner (Answer, page 6), Kuwajima provides a clear teaching of etching a tungsten layer to create a spacer on a via hole to improve the step coverage of conductive fill material. In our view, the skilled artisan, seeking to improve the conductive fill process in Gambino, would clearly be led to combine the teachings of Kuwajima with those of Gambino,

albeit for a different reason than Appellants' intention to prevent dielectric disconnection.

Further, we find compelling evidence in Gambino (column 6, lines 65-67) to support the Examiner's position since it is apparent that Gambino is concerned with the problem of step coverage of conductive fill material. For their part, Appellants assert several arguments which presumably lead to the conclusion that, to whatever extent a step coverage problem exists, Gambino has adequately addressed such problems by using different conductive fill techniques. In the first instance, Appellants point (Brief, page 7) to the discussion at column 8, lines 3-11 of Gambino which discloses the use of a conformal deposition method to ensure "adequate coverage of the bottom of the first opening 320." Secondly, Appellants direct attention to the embodiment illustrated in Figures 21-28 of Gambino and discussed beginning at column 8, line 50 of Gambino. According to Appellants (Reply Brief, page 2), the fact that the tungsten layer is left in the larger contact hole serves to reduce the

step of the larger contact hole, thereby avoiding the need to employ an asserted more complicated etch back process such as in Kuwajima.

We find neither of these arguments of Appellants to be persuasive. A review of the cited portion of Gambino at column 8, lines 3-11 reveals that, although a step coverage problem is addressed, it is directed to the step coverage of insulating material 322 at the bottom of the first opening 320, not the conductive fill material. Further, we find no discussion of the embodiment illustrated in Figures 21-28 of Gambino that mentions any solution to a step coverage concern. In addition, while Appellants suggest that an etch back process is "more complicated" than that employed by Gambino in the Figures 21-28 embodiment, we find no evidence to support such a conclusion.

For all of the above reasons, it is our view that, although Gambino suggests different techniques for applying conductive filler, this does not mitigate the inducement for the artisan to look to techniques, such as the sidewall spacer produced by the tungsten etch back process of Kuwajima, to address the step coverage problem. As the Federal Circuit recently stated,

" . . . this court has consistently stated that a court or examiner may find a motivation to combine prior art references in the nature of the problem to be solved." See Ruiz v. A.B. Chance Co., 357 F.3d 1270, 1274, 69 USPQ2d 1686, 1690 (Fed. Cir. 2004). See also Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996), citing In re Rinehart, 531 F.2d 1048, 1054, 189 USPQ 143, 149 (CCPA 1976) (considering the problem to be solved in a determination of obviousness).

We further find to be unpersuasive Appellants attack (Brief, pages 8-12) on the Examiner's establishment of proper motivation for the proposed combination of Gambino and Kuwajima with the assertion that Kuwajima has no concern with a dielectric disconnection problem since the created tungsten spacer 14c rests on a barrier metal layer 13a, 13b, not a dielectric layer. In a related argument, Appellants contend (id.) that motivation is lacking for the Examiner's suggested combination, since contrary to Kuwajima's created tungsten spacer in the contact hole, Gambino discloses, in the Figures 11-20 embodiment relied upon by

the Examiner, the complete removal of the tungsten layer from the contact hole.

It is apparent to us from the line of reasoning expressed in the Answer, however, that the Examiner is not suggesting the bodily incorporation of Kuwajima's tungsten sidewall spacer into the device of Gambino. Rather, as asserted by the Examiner (Answer, page 17), it is Kuwajima's creation of a tungsten spacer as part of the etch back process to improve conductive fill step coverage in the device of Gambino that is relied upon for the proposed combination. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of [those] references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). See also In re Sneed, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) and In re Nievelt, 482 F.2d 965, 967-68, 179 USPQ 224, 226 (CCPA 1973).

Lastly, while we agree with Appellants that Kuwajima is not concerned with a dielectric disconnection problem, there exists

sufficient motivation for the Examiner's proposed combination with Gambino for other reasons as discussed supra. We also make the observation that the conditions that would lead to dielectric disconnection exist in the integrated circuit manufacturing method disclosed by Gambino for the same reasons as those discussed by Appellants in the background section at pages 1-5 of the specification which discusses the prior art. For example, the etch back removal of the tungsten layer 328 as illustrated in Figure 14 of Gambino creates a condition which would cause a dielectric disconnection upon deposition of dielectric layer 322. In our view, the structure resulting from the combination of Gambino and Kuwajima would solve any dielectric disconnection problem through the creation of the tungsten sidewall spacer.

For the above reasons, since it is our opinion that the Examiner's prima facie case of obviousness has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 103(a) rejection of representative claim 12, as well as claims 14-24, and 26, which fall with claim 12, is sustained.

In summary, we have sustained the Examiner's 35 U.S.C. § 103(a) rejection of all of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 12, 14-24, and 26 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv)(effective September 13, 2004).

AFFIRMED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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JOSEPH F. RUGGIERO) BOARD OF PATENT
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